PCI Express®
Base Specification
Revision 5.0 Version 0.5

November 2, 2017



Note to Reviewers:

We intend to develop and include mechanisms for to support the ability of platforms to select SRIS vs. Non-SRIS modes of Link operation. We are considering the following guiding principles:

1) Typically (but not always), the SRIS vs. Non-SRIS mode will be determined by the form-factor

2) The platform (typically) knows what form-factor(s) is(/are) associated with a particular port

 a. Complications include cases where there are riser cards and "chains" going from one FF to another, e.g. CEM to OCuLink to U.2

3) Si on add-in-cards also typically has some ability to be configured according to the form factor in which it is instantiated

We anticipate developing spec language along these lines:

- Ports that support 32G mode operation must (and others are permitted to) support the SRIS/non-SRIS mode selection mechanism
- Ports that support the mode selection mechanism must support both SRIS and Non-SRIS modes of operation, and must do so such that both the Rx & Tx of the Port are always in the same mode
- The mode selection mechanism will apply at least to all Downstream Ports, and may also apply to Upstream Ports and Retimers

Forward looking comments (please note that these are *not* intended to be limiting statements):

- We expect that the thing selected is the frequency of SKP OS transmission (i.e. it's a Port Tx control knob)
- We intend to consider if we can provide a way for the board level hardware configuration to be detected, although it is not clear if we can do that
- We understand that there may be additional modes of SSC defined, which may in turn add to the list of modes to be selected

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1

1 Introduction

We do not anticipate significant changes in this chapter

2

2 Transaction Layer Specification

Here is a summary of changes being considered in this chapter, some of which may also be included in errata to the PCIe 4.0 Base Specification. All page numbers are in reference to the 4.0.

Page 116: Long list of rules for formation of LN Messages gives no indication of whether receivers should check the rules or not. Add the following after the list. "Receivers may optionally check for violations of these rules (but must not check reserved bits). These checks are independently optional (see Section 6.2.3.4). If a Receiver implementing these checks determines that a TLP violates these rules, the TLP is a Malformed TLP." Note that this is the exact same statement made after the rule list for DRS Message.

Page 171: "Note: The implementation of this optional mechanism is strongly encouraged. Future revisions of this specification may change this mechanism from optional to required." The note refers to an optional flow-control timeout mechanism. Considering making this required for Gen 5.

Page 172: Implementation Note on Flow Control Update Latency – considering removing Table 2-48 and changing the label on Table 2-47 to "Maximum UpdateFC Transmission Latency Guidelines for 8.0 GT/s and Higher Data Rates (Symbol Times)". Note that Table 2-47 and 2-48 are identical and believe the table for 32 GT/s would also be the same.

Errors:

Page 72: reference to Section 2.2.8.5 and 2.2.8.7 is wrong. It should be Section 2.2.8.6.

Page 93: strikeout one occurrence of software in "platform firmware or operating software software that configures PCIe hierarchies to Set the 10-Bit"

Page 105: Last footnote has reference to wrong section. Should be 5.3.3.2.1, not 5.6.4.2.1.

Page 109: Remove "])" from end of the footnote.

Page 113: Add a space between words in "adapteris".

Page 144: "field in those subsequent packets will alw ays indicate the remaining" – remove extra space.

Page 150: "Request it had issued, then a Completion with the Completer Abort Completion" – replace "a" with "it receives a".

Page 152: Last paragraph starting with "Note" should be indented. It applies to the preceding bullet.

Page 177: Some text is upside down in this figure.

Page 183: Bullet item that ends with "down. Otherwise, the following rules apply." – I believe the next 4 bullet items should be indented.

3

3 Data Link Layer Specification

Here is a summary of changes being considered in this chapter, some of which may also be included in errata to the PCIe 4.0 Base Specification. All page numbers are in reference to the 4.0.

Page 197: Change "All Ports are permitted to support Scaled Flow Control. Ports that support 16.0 GT/s must support Scaled Flow Control. Scaled Flow Control activation does not affect the ability to operate at 16.0 GT/s." to "All Ports are permitted to support Scaled Flow Control. Ports that support 16.0 GT/s or higher data rates must support Scaled Flow Control. Scaled Flow Control activation does not affect the ability to operate at 16.0 GT/s or higher data rates."

Errors

Page 197: "account for t he Link round trip time" should be "account for the Link round trip time".

4

4 Physical Layer Logical Block

The Physical Layer will follow the 128b/130b encoding when operating at 32.0 GT/s Data Rate.

The 32.0 GT/s Data Rate will be backwards compatible with the prior Data Rates. Thus, the Link will train to L0 in 2.5 GT/s and then move to the higher Data Rate(s). The TS1 and TS2 Ordered Sets in 8b/10b encoding as well as 128b/130b encoding will be enhanced to include the 32.0 GT/s Data Rate support (Symbol 4, Bit 5).

The equalization flows will be similar to the 8.0 GT/s and 16.0 GT/s Data Rate equalization flows. After training to L0 in 2.5 GT/s, the Link will perform equalization at 8.0 GT/s, followed by 16.0 GT/s equalization, followed by equalization at 32.0 GT/s.

Optimizing the Link to skip (or reorder) equalization at lower Data Rates when supporting 32.0 GT/s Data Rate will be allowed as an optional feature. This will be negotiated during Configuration.Lanenum.Wait, Configuration.Lanenum.Accept, and Configuration.Complete substates through the exchange of modified TS1/TS2 Ordered sets in 8b/10b encoding as the link initially trains to L0. The capability to send and received these modified Ordered Sets are exchanged during Polling, Configuration.Linkwidth.Start, and Configuration.Linkwidth.Accept (sub)states by setting the bit 7 of Symbol 5 of the standard TS1 Ordered Sets to 1b.

In addition to the decision to skip equalization, alternate protocols can also be negotiated during the Configuration.Lanenum.Wait, Configuration.Lanenum.Accept, and Configuration.Complete substates through the exchange of modified TS1/TS2 Ordered sets in 8b/10b encoding.

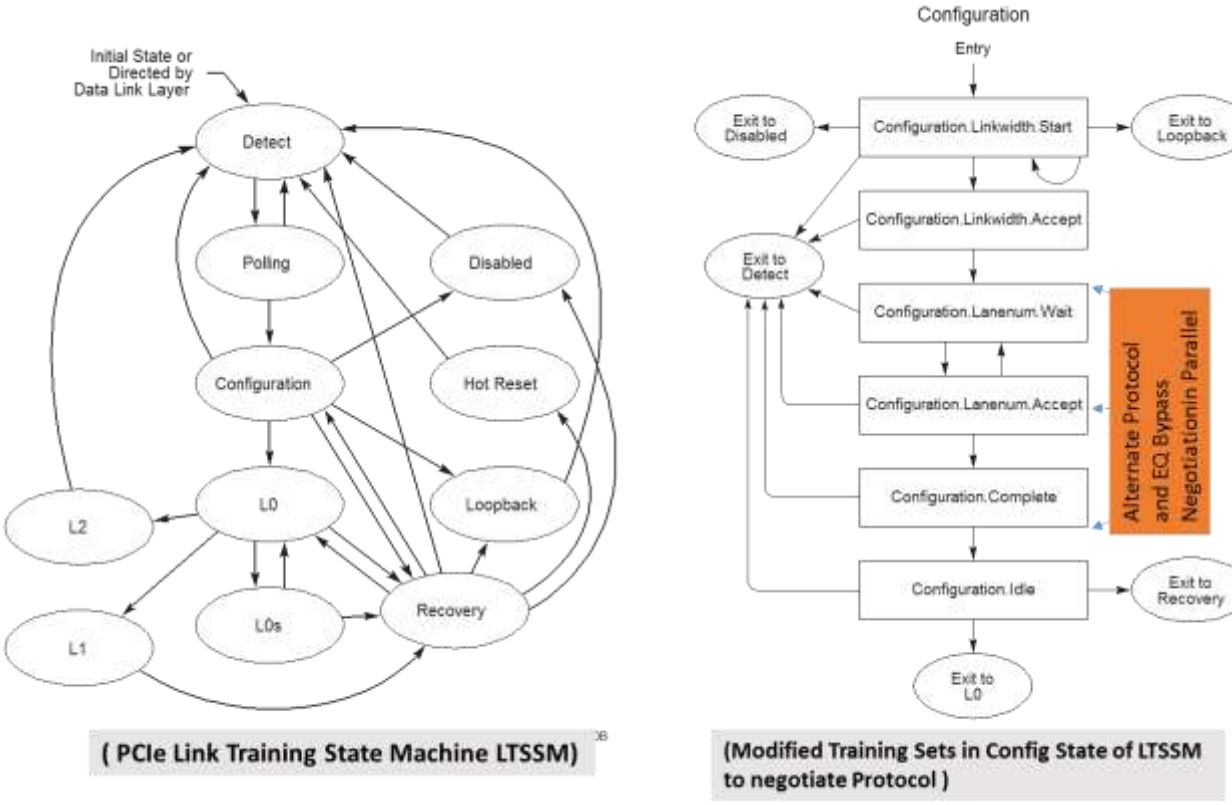
The following table describes Modified TS1/TS2 Ordered Sets:

Symbol No	Standard TS1/ TS2 (EQ TS1/ TS2)	Modified TS1/ TS2
0	COM	COM
1	Link Number	Link Number
2	Lane Number	Lane Number
3	N_FTS	N_FTS
4	Data Rate Identifier	Data Rate Identifier
5	Training Control Bit 0 - Hot Reset Bit 1 - Disable Link Bit 2 - Loopback Bit 3 - Disable Scrambling	Training Control Bit 4:0 – 00001b: Hot Reset 00010b: Disable Link 00100b: Loopback

	Bit 4 - Compliance Receive Bit 5 – Reserved Bit 6 – Reserved Bit 7 – In Polling and Configuration.Linkwidth.Start and Configuration.Linkwidth.Accept substates while Link_Up=0b: Modified TS1/TS2 supported when 1b; Modified TS1/TS2 not supported when 0b Other states: Reserved	01000b: Disable Scrambling 10000b: Compliance Receive Bit 5 - Reserved Bit 6 – In Configuration State: Support for Equalization at the highest common Data Rate only when set to 1b; Reserved in other states Bit 7 = 1b
6	D10.2 for Standard TS1 EQ TS1: Bit 2:0 – Rx preset Hint Bit 6:3: Tx Preset Bit 7: Set to 1b	If Bit 7 is 0b Bit 6:0 : Reserved for future usage Else Bit 2:0 – Rx preset Hint Bit 6:3: Tx Preset
7	D10.2 or D5.2	D10.2 or D5.2
8	D10.2 or D5.2	D10.2 or D5.2
9	D10.2 or D5.2	Bit 1:0 - Usage 00b: Alternate Protocols 01b, 10b: Reserved 11b: Vendor Defined usage Bit 15:2: If Usage = 00b: • Bit 15:14: Alternate protocol negotiation status: o 00b: Alternate protocol request (DSP); Evaluating the Alternate protocol request (USP) – Alternate Protocol Details bits all 0s when it has not received at least 2 consecutive TS1'es with the same protocol details o 01b: Alternate protocol accept for USP (the details reflect what was sent by DSP) 1. Reserved for DSP o 10b: Reject alternate protocol negotiation and propose new alternate protocol for USP, if available or have the Alternate Protocol Details field as all 0s if it does not want to propose a new protocol 2. Reserved for DSP o 11b: Reserved • Bit 13:2: Alternate Protocol Details Else Reserved
10	D10.2 or D5.2	

11	D10.2 or D5.2	Bit 15:0: Vendor/ Protocol ID
12	D10.2 or D5.2	
13	D10.2 or D5.2	Bit 15:0: Proprietary bits based on "Usage" field in Symbol 9
14	D10.2 or D5.2	
15	D10.2 or D5.2	Bit-wise even parity of Symbols 9-14

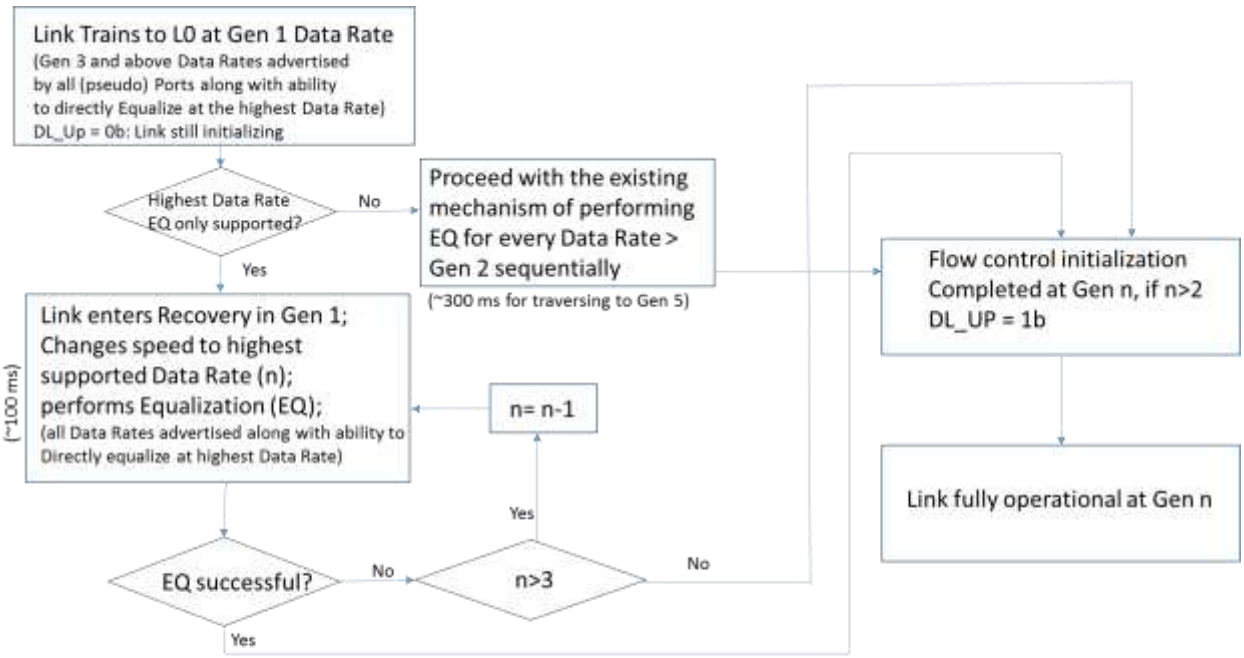
The following diagram represents the states where alternate protocol and equalization bypass negotiation occurs:



(PCIe Link Training State Machine LTSSM)

(Modified Training Sets in Config State of LTSSM to negotiate Protocol)

The following flow-chart provides an example flow where a Link may bypass equalization at lower Data Rates and go to the highest support data rate for equalization.



The ElEOS Ordered set in 128b/130b encoding may be modified to include longer run length of 0s and 1s (e.g., alternate between 32 0b and 32 1b) if our analysis shows that the 16.0 GT/s EIEOS does not meet the electrical idle exit requirements at 32.0 GT/s Data Rate.

The compliance patterns are expected to be identical to the 16.0 GT/s Data Rate, subject to analysis of the pattern at 32.0 GT/s Data rate. At 32.0 GT/s, another 19 sets of patterns with various presets will be added, similar to the 19 sets of patterns that were added for 16.0 GT/s Data Rate.

We are expecting Lane Margining at Receiver to remain unchanged at 32.0 GT/s Data Rate.

The maximum number of re-timers is not expected to change from 2 to support the 32.0 GT/s Data Rate.

We are expecting to have a new extended capability structure for 32.0 GT/s Data Rate and several register fields will be expanded to accommodate the 32.0 GT/s Data Rate.

Open for Rev 0.5: We will likely change the SKP OS encoding for 32GT/s data rate so that it does not result in the clock pattern, as we have now. Subject to circuit/ channel simulations, we may also include a simple "precoding" scheme where bit (n) at the transmitter is the XOR of bin (n) and bit (n-1) and the inverse is applied for decode at the receiver. This will be done in conjunction with the scrambler. This will most likely be an optional feature for the Receiver to ask (but the Transmitter must do precoding if asked) that will be turned on at 32GT/s Data Rate, subject to TS1/TS2 negotiation prior to entering 32 GT/s Data Rate, on a per Link segment direction basis, only under certain channel for certain types of Receivers. The SKP OS encoding will likely change from the existing clock pattern for 32 GT/s. This will be resolved by the Spec Rev 0.7.

5

5 Power Management

5 *We do not anticipate significant changes in this chapter*

6

6 System Architecture

We do not anticipate significant changes in this chapter

7

7 Software Initialization and Configuration

Insert two new sections into Chapter 7 – Note that these new sections will probably be integrated as Sections 7.7.8 and 7.7.9

7.1. Physical Layer 32.0 GT/s Extended Capability

Warning : This capability is under active development. This material will likely change, perhaps significantly, in the next release of this specification.

The Physical Layer 32.0 GT/s Extended Capability structure must be implemented in:

- A Function associated with a Downstream Port where the **Error! Reference source not found.** field indicates support for a Link Speed of 32.0 GT/s.
- A Function of a single-Function Device associated with an Upstream Port where the **Error! Reference source not found.** field indicates support for a Link Speed of 32.0 GT/s.
- Function 0 (and only Function 0) of a Multi-Function Device associated with an Upstream Port where the **Error! Reference source not found.** field indicates support for a Link Speed of 32.0 GT/s.

This capability is permitted to be implemented in any of the Functions listed above even if the 32.0 GT/s Link Speed is not supported. When the 32.0 GT/s Link Speed is not supported, the behavior of registers other than the Capability Header is undefined.

Figure 7-1 details allocation of register fields in the Physical Layer 32.0 GT/s Extended Capability structure.

Issue 1) Create 32.0 GT/s Physical Layer Extended Capability Figure
(same as 16.0 GT/s figure removing the 3 Data Parity registers)

Figure 7-1: Physical Layer 32.0 GT/s Extended Capability

7.1.1. Physical Layer 32.0 GT/s Extended Capability Header (Offset 00h)

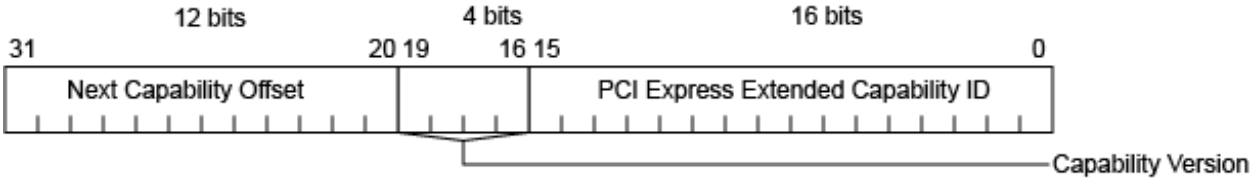


Figure 7-2: Physical Layer 32.0 GT/s Extended Capability Header

Table 7-1: Physical Layer 32.0 GT/s Extended Capability Header

Bit Location	Register Description	Attributes
15:0	*Physical Layer 32.0 GT/s PCI Express Extended Capability ID* – This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Physical Layer 32.0 GT/s Capability is **TBD**. Issue 2) Assign Extended Capability ID.	RO
19:16	*Physical Layer 32.0 GT/s Capability Version* – This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	*Physical Layer 32.0 GT/s Next Capability Offset* – This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	RO

7.1.2. Physical Layer 32.0 GT/s Capabilities Register (Offset 04h)

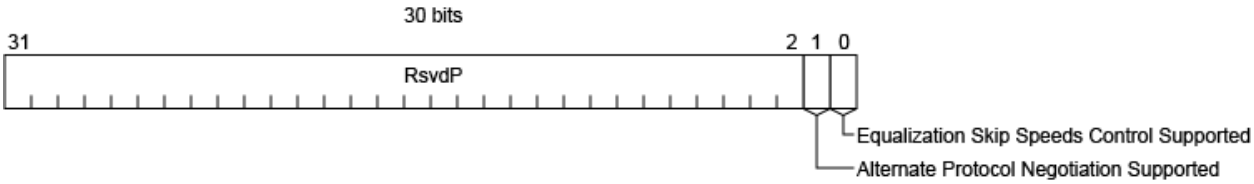


Figure 7-3: Physical Layer 32.0 GT/s Capabilities Register

Table 7-2: Physical Layer 32.0 GT/s Capabilities Register

Bit Location	Register Description	Attributes
0	*Equalization Skip Speeds Control Supported* - When Set, this Port supports controlling whether the Port negotiates to skip equalization for speeds other than the highest common supported speed. See Section **4.TBD** for details.	HwInit

	Must be 1b for Ports that support 32.0 GT/s or higher data rates. Issue 3) Fix reference to **4.TBD**.	
1	*Alternate Protocol Negotiation Supported* - When Set, this Port supports negotiating to use alternate protocols on one or more Lanes of this Link. When Clear, this Port does not support use of alternate protocols on any Lane of this Link. See Section **4.TBD** for details. Default is Implementation Specific. Issue 4) Fix reference to **4.TBD**.	HwInit

7.1.3. Physical Layer 32.0 GT/s Control Register (Offset 08h)

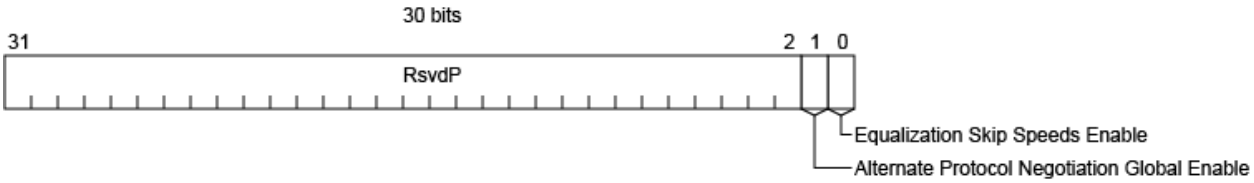


Figure 7-4: Physical Layer 32.0 GT/s Control Register

Table 7-3: Physical Layer 32.0 GT/s Control Register

Bit Location	Register Description	Attributes
0	*Equalization Skip Speeds Enable* - When Set, this Port indicates during Link Training that is wishes to train to the highest common link data rate and skip equalization of intermediate data rates. See Section **4.TBD** for details. If *Equalization Skip Speeds Control Supported* is Set, this bit is RWS with a default value of 1b. If *Equalization Skip Speeds Control Supported* is Clear, this bit is permitted to be hardwired to 0b. Issue 5) Fix reference to **4.TBD**.	RWS/HwInit
1	*Alternate Protocol Negotiation Global Enable* - When Set, this Port is enabled to negotiate to use alternate protocols on one or more Lanes of this Link. When Clear, this Port is not enabled to negotiate use of alternate protocols on any Lane of this Link. See Section **4.TBD** for details. This bit is permitted to be hardwired to 0b if *Alternate Protocol Negotiation Supported* is Clear. Behavior is undefined if this bit is Set and *Alternate Protocol Negotiation Supported* is Clear. More detailed control of Alternate Protocol Negotiation is possible by using the optional ***Error! Reference source not found.*** field. Default is Implementation Specific.	RWS/RO

Issue 6) Fix reference to **4.TBD**.

7.1.4. Physical Layer 32.0 GT/s Status Register (Offset 0Ch)

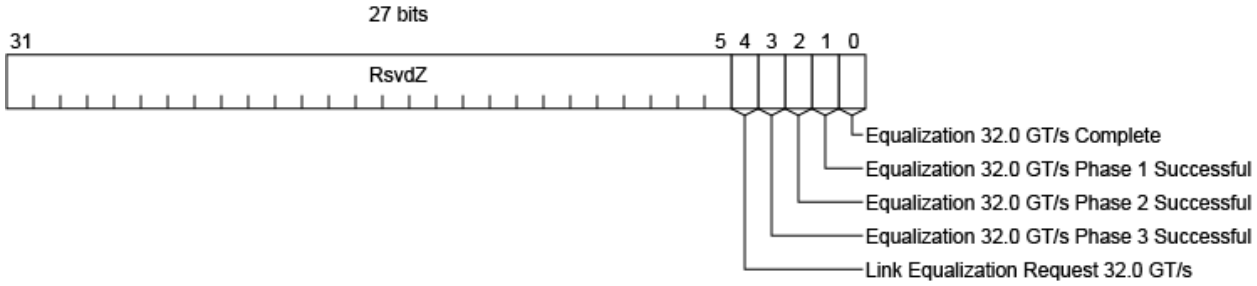


Figure 7-5: Physical Layer 32.0 GT/s Status Register

Table 7-4: Physical Layer 32.0 GT/s Status Register

Bit Location	Register Description	Attributes
0	*Equalization 32.0 GT/s Complete* – When Set, this bit indicates that the 32.0 GT/s Transmitter Equalization procedure has completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section **Error! Reference source not found.**. The default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.	ROS/ RsvdZ
1	*Equalization 32.0 GT/s Phase 1 Successful* – When set to 1b, this bit indicates that Phase 1 of the 32.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section **Error! Reference source not found.**. The default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.	ROS/ RsvdZ
2	*Equalization 32.0 GT/s Phase 2 Successful* – When set to 1b, this bit indicates that Phase 2 of the 32.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section **Error! Reference source not found.**. The default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.	ROS/RsvdZ
3	*Equalization 32.0 GT/s Phase 3 Successful* – When set to 1b, this bit indicates that Phase 3 of the 32.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section **Error! Reference source not found.**. The default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in	ROS/RsvdZ

	Function 0 and RsvdZ in other Functions.	
4	*Link Equalization Request 32.0 GT/s* – This bit is Set by hardware to request the 32.0 GT/s Link equalization process to be performed on the Link. Refer to Section **Error! Reference source not found.** and Section **Error! Reference source not found.** for details. The default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.	RW1CS/RsvdZ

7.1.5. Physical Layer 32.0 GT/s Reserved Register (Offset 1Ch)

This register is RsvdP.

7.1.6. Physical Layer 32.0 GT/s Lane Equalization Control Register (Offset 20h)

The *Physical Layer 32.0 GT/s Equalization Control* register consists of control fields required for per-Lane 32.0 GT/s equalization. It contains entries for at least the number of Lanes defined by the **Error! Reference source not found.** field (see Section **Error! Reference source not found.**), must be implemented in whole DW size increments, and it is permitted to contain up to 32 entries regardless of **Error! Reference source not found.**. The value of entries beyond **Error! Reference source not found.** is undefined.

Issue 7) Locate artwork (same as 16.0 GT/s figure)

Figure 7-6: High Level Structure of 32.0 GT/s Lane Equalization Control Register

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.

Warning : There is ongoing discussion as to whether or not the 32.0 GT/s Link Speed uses Precoding. Precoding is a mechanism that, is thought to reduce the probability of large burst errors occurring for certain data patterns (after scrambling). It is postulated that, for some receivers on some channels, the probability of large burst errors may increase when compared to previous designs and the large burst errors may not be caught by the existing CRC mechanism.

If Precoding is adopted, a 1-bit *Upstream Port 32.0 GT/s Precoding Enable* field may be added to each *Lane Equalization Control Register Entry*.



Figure 7-7: 32.0 GT/s Lane Equalization Control Register Entry

Table 7-5: 32.0 GT/s Lane Equalization Control Register Entry

<table>
<tr><th>Bit Location</th><th>Register Description</th><th>Attributes</th></tr>
<tr><td>3:0</td><td>Downstream Port 32.0 GT/s Transmitter Preset – Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. See Error! Reference source not found. for details. The field encodings are defined in Section Error! Reference source not found..
For an Upstream Port if Error! Reference source not found. is 0b, this field is RsvdP. Otherwise, this field is HwInit. See Section Error! Reference source not found..
The default value is 1111b.</td><td>HwInit/RsvdP (see description)</td></tr>
<tr><td>7:4</td><td>Upstream Port 32.0 GT/s Transmitter Preset – Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization. Field usage varies as follows:
<table>
<tr><th></th><th>Operating Port Direction</th><th>Error! Reference source not found.</th><th>Usage</th></tr>
<tr><td>A</td><td>Downstream Port</td><td>Any</td><td>Field contains the value sent on the associated Lane during Link Equalization.
Field is HwInit.</td></tr>
<tr><td>B</td><td>Upstream Port</td><td>0b</td><td>Field is intended for debug and diagnostics. It contains the value captured from the associated Lane during Link Equalization.
Field is RO.
When crosslinks are supported, case C (below) applies and this captured information is not visible to software. Vendors are encouraged to provide an alternate mechanism to obtain this information.</td></tr>
<tr><td>C</td><td>Upstream Port</td><td>1b</td><td>Field is not used or affected by the current Link Equalization.</td></tr>
</table></td><td>HwInit/RO (see description)</td></tr>
</table>

				Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A (above) applies. Field is HwInit.
	See Section **Error! Reference source not found.** and **Error! Reference source not found.** for details. The field encodings are defined in Section **Error! Reference source not found.**. The default value is 1111b.			

7.2. Alternate Protocol Extended Capability

Warning :

The Alternate Protocol Negotiation mechanism is under active development. This material is forward looking and reflects current thinking and direction. This material will likely change, perhaps significantly, in the next release of this specification.

We anticipate the need to ask a Port about supported Alternate Protocols, control mechanisms for Downstream Ports, potentially with some Lane subset selection capability.

The Alternate Protocol Extended Capability structure is optional. It is associated with a Link, and is only permitted in:

- A Function associated with a Downstream Port.
- Function 0 (and only Function 0) of a Device associated with an Upstream Port.

See Chapter 4 for more information regarding the Phy-Logical mechanisms for Alternate Protocols.

8

8 Electrical Sub-Block



5.0 Rev 0.5 Slides

Updated October 5, 2017

PCI-SIG® EWG

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5.0 Tx Jitter Parameters

		2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	
T_{TX-UTJ}	Tx uncorrelated total jitter	100 (max)	50 (max)	31.25 (max)	12.5 (max)	**6.25 (max)**	ps PP at 10-12
$T_{TX-UTJ-SRIS}$	Tx uncorrelated total jitter when testing for the IR clock mode with SSC	100 (max)	66.51 (max)	33.83 (max)	15.85 (max)	**7.93 (max)**	ps PP at 10-12
$T_{TX-UDJDD}$	Tx uncorrelated Dj for non-embedded Refclk	100 (max)	30 (max)	12 (max)	6.25 (max)	**3.125 (max)**	ps PP
$T_{TX-UPW-TJ}$	Total uncorrelated pulse width jitter	N/A	40 (max)	24 (max)	12.5 (max)	**6.25 (max)**	ps PP at 10-12
$T_{TX-UPWDJDD}$	Deterministic DjDD uncorrelated pulse width jitter	N/A	40 (max)	10 (max)	5 (max)	**2.5 (max)**	ps PP
T_{TX-RJ}	Tx Random jitter	N/A	1.4 – 3.6	1.4 – 2.2	0.45 – 0.89	**.23 - .45**	ps RMS

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SRIS and Common Clock

- **PCIe 5.0 base specification compliant PHYs must support both common clock and SRIS clocking architectures. Form factor specifications can still decide their clocking requirements.**
- **The following PPM changes are for SRIS – there are no changes in requirements for common clock**
 - The maximum transmitted SSC PPM in SRIS for 5.0 compliant devices that advertise support for 32 GT/s at all data rates is a down spread of 1000 PPM.
 - The maximum transmitted SSC PPM in SRIS for 5.0 compliant devices that do not advertise support 32 GT/s at all data rates is a down spread of 5000 PPM.
 - A 5.0 32 GT/s device capable still needs to support receiving up to 5000 ppm down spread from the link partner at speeds below 32 GT/s.

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PCIe 5.0 Reference Clock

Data Rate	CC jitter Limit	Notes
2.5 GT/s	86 ps pp	1, 2
5.0 GT/s	3.1 ps RMS	1, 2
8.0 GT/s	1.0 ps RMS	1, 2
16.0 GT/s	≤0.5 ps RMS	1, 2, 3, 4
32 GT/s	≤0.25 ps RMS	1,2,3,5, 6

Table 9-22: Jitter Limits for CC Architecture

Notes:

1. The Refclk jitter is measured after applying the filter function in Figure 9-52
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real time oscilloscope with a sample rate of 20 GS/s or great. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation).
3. For the 16.0 GT/s and 32 GT/s CC measurement the SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7 ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that .35 ps RMS is to be used in channel simulations to account for additional noise in a real system with PLL limits of 1.25 and 2.5 MHz and a model CDR with a 20 Mhz bandwidth.
6. Alternate measurement methodologies are being studied and the methodology could be changed in the .7 specification. It is possible a different measurement methodology could impact the specification limits and/or CDR and PLL specifications.

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Reference Clock

- **The PPM limit for the reference clock is reduced from 300 ppm to 100 ppm**

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5.0 Common Clock PLL Requirements

- **The common clock PLL limits at 32 GT/s are 1.25 to 2.50 MHz**
- **The common clock reference CDR at 32 GT/s is 20 MHz first order**
- **A 5.0 base specification compliant device when operating at 8.0 or 16 GT/s must follow either:**
 - PCIe 4.0 specification requirements for PLL bandwidth and Tx jitter at 8.0 and 16.0 GT/s
 - PCIe 5.0 specification requirements for PLL bandwidth and Tx at 8.0 and 16.0 GT/s as follows:
 - 16 GT/s - T_{TX-UTJ} = 11.8 ps
 - 16 GT/s - T_{TX-RJ} = .40 - .84 ps RMS
 - 8 GT/s - T_{TX-UTJ} = 30.55 ps
 - 8 GT/s - T_{TX-RJ} = 1.29 – 2.18 ps RMS
 - Note – only the Tx jitter limits that change are shown – all other Tx jitter limits at 8.0 and 16.0 GT/s remain the same
 - Note – these measurements are still performed with the PCIe 4.0 specification reference CDR for 16 GT/s

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Reference Equalizer

- **CTLE**
 - Pole 1 – 4 GHz
 - Pole 2 – 32 GHz
 - -5 to -15 dB DC Gain
 - Alternate CTLE options that better match the inverse of a typical channel response are being studied and it is likely the reference CTLE will be improved for .7 specification.
- **DFE**
 - 6 taps
 - 20 mV maximum tap weight
 - The 20 mV maximum was used to indirectly limit the H1/H0 ratio with maximum loss channels. As more analysis is done for the .7 specification, including quantifying the benefit of precoding - this limit and/or the number of taps could change
- **CDR Offset**
 - -.3 UI max with a .05 UI step size from the sample position at the mean of the edges – picking the offset that gives the largest eye area
 - Note – alternate figures of merit than eye area will be considered for the .7 revision of the specification
- **No AC Gain**
- **Eye Target at pad for channel compliance**
 - 7.5 mV pp and .3 UI pp
- **Current Direction – Likely needs additional improvement in the reference CTLE for sufficient margins over HVM with 36 dB channels.**
 - No change to DC gain range expected – just better shaping/matching of typical channel inverse
 - Alternate CTLE proposals will be studied for inclusion in the .7 specification

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H1/H0 text for .5

- **In PCI Express 5.0 receiver operation at 32 GT/s a large DFE tap 1 weight (H1) to main cursor (H0) ratio increases the risk that a bit error can result in an error burst that is not handled by the CRC. The PCI-SIG electrical workgroup is considering standardizing one or both of the following two options:**
- **1) Having the PCIe 5.0 behavioral receiver definition directly limit the H1/H0 ratio to less than .7.**
- **2) Adding precoding to the standard so a receiver using a large H1/H0 ratio can optionally cause the transmitter of the link partner to transmit the XOR of bit n and coded bit n-1 to reduce the risk of a random error propagating (see TBD reference to Phy Logical chapter). Precoding use is optional for the receiver and the capability is required for the transmitter.**
- **Please provide feedback on this for the next revision of the specification.**

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Reference Packages and Channel Compliance

- **PCIe 5.0 reference packages for 32 GT/s channel simulations and stressed eye test calibration will be normative**
- **The rev .5 specification provides insertion loss and cross-talk limits for 5.0 packages. The .7 specification will provide reference models**
- **The package insertion loss limits (including cpad) are:**
 - Root – 9.0 dB at 16 GHz (including socket)
 - Non-root – 4.0 dB at 16 GHz
- **The package models for the .7 specification must include realistic NEXT cross-talk from the sum of all aggressors**
 - The strongest next aggressor in the package is recommended to be less than -55 dB
- **The .7 specification will include package aggregate NEXT and FEXT frequency masks**
- **The pad to pad insertion loss target for channel compliance is 36 dB at 16 GHz for typical channels containing up to 2 connectors**

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Other .5 Topics

- **EIEOS when transmitting at 32 GT/s will be 32 repeating ones and zeroes (still 16 at 16 GT/s)**
 - Increasing the number blocks is under consideration for the next revision of the specification

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&
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9 SR-IOV // 10 ATS Specification

We do not anticipate significant changes in this chapter or to the appendices

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